NL 010168
US#4

Europäisches Patentamt
European Patent Office
Office européen des brevets

Bescheinigung Certificate Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

01200874.4

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

DEN HAAG, DEN
THE HAGUE, 29/01/02
LA HAYE, LE

Europäisches Patentamt
European Patent Office
Office européen des brevets

Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

Anmeldung Nr.:
Application no.: 01200874.4
Demande n°:

Anmeldetag:
Date of filing: 08/03/01
Date de dépôt:

Anmelder:
Applicant(s):
Demandeur(s):
Koninklijke Philips Electronics N.V.
5621 BA Eindhoven
NETHERLANDS

Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
Enhanced reduced pin-count test for full-scan design

In Anspruch genommene Priorität(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

Staat: State: Pays:	Tag: Date: Date:	Aktenzeichen: File no. Numéro de dépôt:

Internationale Patentklassifikation:
International Patent classification:
Classification internationale des brevets:
/

Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

Enhanced Reduced Pin-Count Test for Full-Scan Design

Abstract

This invention is related to enhanced reduced pin-count test (RPCT) for low-cost test. Enhanced RPCT is an extension of traditional RPCT for circuits on which a large number of digital IC pins is multiplexed for scan. The basic concept of enhanced RPCT is to provide access to the internal scan chains via an IEEE 1149.1 compatible boundary-scan architecture, instead of direct access via the IC pins. The boundary-scan chain performs serial/parallel conversion of test data. Enhanced RPCT also provides I/O wrap to test non-contacted pins. The invention also relates to enhanced RPCT for full-scan design, as well as for full-scan core-based design.

1. Introduction

The costs of IC testing and particularly the cost of automated test equipment (ATE) are major concerns for semiconductor industry. The SIA International Technology Roadmap for Semiconductors (ITRS) predicts that the cost of high-end ATE for full-pin, at-speed, functional testing may rise to $20M-$50M in ten years time [1]. The ITRS shows that the cost per pin for high-end ATE has remained essentially flat for the past 20 years at $10K–$12K/pin. Although this cost has decreased since 1999 below $8K/pin, it is expected that future demands on higher speed, greater accuracy, more time sets, increased vector memory, and higher pin-counts will offset all the gains for reducing ATE cost.

The general feeling is that incorporating more design-for-testability (DFT) into IC designs is the only way to reverse the trend of rising ATE costs and to enable the use of low-cost ATE. Low-cost ATE offers reduced capabilities, which are suited for structural testing but insufficient for functional testing. High test quality with low-cost ATE can therefore only be obtained if ICs are equipped with DFT which provides high fault coverage with structural testing. Some semiconductor companies have stated that their quality levels have even improved after introducing low-cost ATE, since this enforced them to enhance their DFT methods [2].

Low-cost ATE is typically meant for production testing, while high-end ATE is still required for tasks as device characterization and diagnostics. The general approach is that low-cost ATE is introduced first during wafer testing, while high-end ATE is still used during final test after the IC has been packaged. However, some companies have already reported the use of low-cost ATE during both wafer test and final test, without experiencing loss of quality [2].

The cost reduction in low-cost ATE is mainly achieved due to the following reasons:

- Traditional ATE uses expensive, high-speed vector memory. Low-cost ATE allows to use cheap, low-speed memory for storing test vectors, e.g. commodity DRAM as used in PCs or hard-disks.
- In general, less than 5 tester channels are required for high speed, high accuracy clock and control signals, and only these channels require high-performance pin electronics.
- Digital data pins (i.e. functional I/O pins) require only low-speed tester channels with high timing accuracy. The complexity of the pin electronics for these pins can be reduced further by restricting the number of waveform shapes, voltage range, and the number of timing edges.
- All dedicated scan pins (i.e. dedicated I/O pins for scan data input or output) require only low-speed tester channels with low timing accuracy.
- High-end testers allow to test both logic, memory, and analog parts that reside on a system-on-chip (SOC). Particularly testing of analog parts puts constraints on the ATE, such as a low overall noise floor. The focus of low-cost ATE on short term is therefore on digital only.

This invention introduces enhanced reduced pin-count test (RPCT) as an enabling DFT technique for low-cost test. In RPCT, only the IC pins for scan in/out, clocks, control, power and ground, and possibly analog pins are contacted by the tester, while all functional I/O pins are accessed via the boundary-scan chain instead of direct access via the pins. RPCT only pays off if the amount of functional I/O pins is substantial. Within Philips, it is however common practice to optimize test time by using many parallel scan chains. Every digital IC pin is therefore multiplexed for scan, and a design contains as many scan chains as pin-count allows. In this situation, traditional RPCT cannot be applied since all pins are used for scan and have to be contacted by the tester. This paper introduces enhanced RPCT, which implements serial/parallel conversion of scan data and provides that not all scan pins have to be contacted by the tester.

The remainder of this document is organized as follows. An overview of DFT and low-cost ATE is provided in

Section 2, and the state-of-the-art on traditional RPCT is described in Section 3. Enhanced RPCT for full-scan design is presented in Section 4, and Section 5 describes enhanced RPCT for core-based design. Tooling issues are discussed in Section 6.

2. DFT and Low-Cost ATE

Low-cost ATE requires the use of additional DFT to achieve high fault coverage with structural testing. Examples of key DFT techniques for low-cost ATE are built-in self-test (BIST) and test data compression. These techniques reduce the test data volume which has to be stored in the ATE vector memory, and they also relax the bandwidth problem as caused by transporting test data between the ATE and the IC over a limited number of pin channels at a relatively low speed. Transporting large amounts of test data with limited bandwidth results in large test application time.

BIST implies that test stimuli are generated on-chip, and that test responses are evaluated on-chip. BIST provides various advantages for low-cost testing. It allows to execute tests at high, on-chip frequencies. Even a complex SOC can be tested on a low-cost ATE when applying dedicated BIST schemes for logic, memories, and analog blocks. Furthermore, BIST reduces the test data volume in ATE vector memory to an absolute minimum. Only few clock and control signals are required to execute the test and BIST therefore provides an excellent solution to the bandwidth problem [3]. BIST is already widely used for testing large embedded memories, while BIST for random logic and analog blocks is emerging. However, BIST requires some additional silicon area. Although silicon area itself is no longer considered as a major cost factor for many ICs, silicon area is often a scarce resource in semiconductor fabs that are operating closely to their maximum production capacity.

DFT for test data compression is a hybrid form between BIST and external testing, e.g. [4][5][6][7]. The basic principle is to store test stimuli in the ATE vector memory in a compressed format, and to transfer these compressed stimuli to the IC via a limited number of tester channels. The IC requires special circuitry to decompress the stimuli. The test responses can easily be compressed on-chip using one or more on-chip MISRs (multiple-input signature register). Test data compression relaxes the bandwidth problem, while the silicon area for the compression/-decompression circuitry is rather small.

Some semiconductor companies (e.g. IBM [8][9]) are using older, amortized ATE as low-cost ATE. The vector memory in this low-cost ATE can only be extended slightly, and growing test data volume is therefore a major concern. However, it is expected that the upcoming low-cost ATE will use cheap DRAM or hard-disks as vector memory, and consequently the test data volume on itself will no longer be a concern. The bandwidth problem is of more concern, and requires DFT techniques such as BIST or test data compression. Furthermore for mixed-signal devices, the test application time for the analog parts is usually orders of magnitude larger than the application time for the digital parts, and a slight increase in the digital test time may be tolerated. Although BIST and test data compression are ultimate DFT techniques for dealing with test data volume and bandwidth problems, they may not yet be economically feasible on many products.

Reduced pin-count test (RPCT) is a DFT technique to reduce the number of IC pins that have to be contacted by the tester. Although RPCT does not address directly test data volume reduction or the bandwidth problem, it is a key technique for low-cost, high-quality test. RPCT enables the use of relatively low-cost testers that contain fewer full-functional pin channels than the number of I/O pins on the device being tested. RPCT enables the use of simpler probe cards, and it provides that yield loss due to bad contacting and tester inaccuracy is reduced. Furthermore, contacting less IC pins enables multi-site or parallel testing, which provides that a tester can test multiple ICs in parallel. Multi-site testing is generally seen as one of the most important techniques to reduce test costs. The ITRS predicts that the number of sites tested in parallel will increase from 2-4 to 8-32 [1].

RPCT is not only useful for testing on low-cost ATE with limited capabilities, but also in general to test ICs with large pin-counts. Testing new ICs with large pin-counts may not be possible on currently available ATE, and requires either extending current ATE or installing new ATE.

3. Reduced Pin-Count Test

IBM has reported on RPCT with LSSD boundary scan to enable the use of low-cost ATE for ASICs [8][9][10] and S/390 microprocessors [11][12]. Also TI has presented the use of DFT and RPCT to test devices with several thousands of I/O pins on low-cost ATE of only $200/pin. RPCT requires that the IC is a full-scan design and incorporates boundary-scan functionality. As shown in Figure 1, the basic principle of RPCT is that only scan data pins (i.e. input and output pins of the scan chains, and TDI and TDO of the boundary-scan chain), test control pins, and clock pins are connected to full-functional tester channels. Access to all remaining functional pins is achieved via the boundary-scan chain, instead of direct access via the pins. An alternative to access via the boundary-scan chain is e.g. access via a dedicated surround chain or test points.

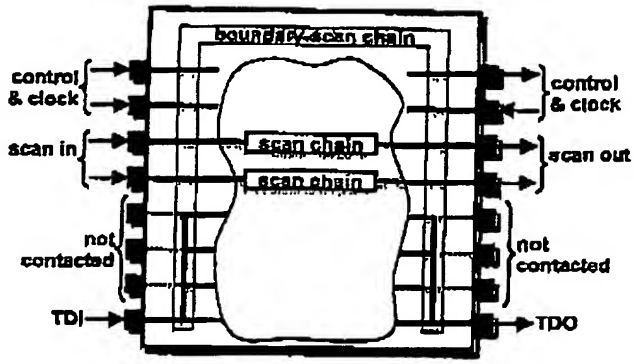

Figure 1: Reduced pin-count test

RPCT can be implemented using a boundary-scan architecture compatible to the IEEE 1149.1 standard [13]. However, several extensions are required. The boundary-scan chain should operate during RPCT as a regular scan chain, so that the boundary-scan chain and the internal scan chains can be loaded/unloaded simultaneously. Furthermore, the boundary-scan cells at the clock and control pins should be transparent during RPCT, and also the scan pins should be transparent during RPCT for direct access to the internal scan chains.

RPCT can be used both at wafer test and at final test after packaging. A typical scenario is to use RPCT first at wafer test, where all functional I/O pins are not probed and not contacted by the tester. RPCT is used next at final test, and now the functional I/O pins are contacted by simple DC-parametric channels for contact tests and parametric tests. The problem with this scenario is that the I/O circuitry of the pins is not tested during wafer test. This results in lower test quality during wafer test, and a fault in the pin I/O circuitry is only detected after packaging during final test.

A solution is to use a technique known as I/O wrap. Every non-contacted pin is implemented as a bidirectional pin, independent of functional requirements. A functionally input-only pin can be turned into an I/O pin by adding a small driver, just strong enough to drive the receiver. During testing a loop-back path is created from the boundary-scan cell in front of the output buffer into the boundary-scan cell after the input buffer. Hence, the test signal wraps back into the chip rather than being observed outside on the IC pin. The I/O wrap tests the circuitry between the boundary-scan chain and the bonding pads. What remains untested are the connection from the pin to the bonding-pad, the connections from the pad to the driver and receiver, the functional path from the pad into the chip, and whether the driver and receiver can actually drive and receive valid voltage and current levels. These issues are tested during DC-parametric tests at final test.

IBM has reported the use of I/O wrap in combination with RPCT. Initially, I/O wrap was used to perform static tests for detecting stuck-at faults [10], while recently I/O wrap has been extended to perform delay fault testing of I/O circuits [14]. I/O wrap for delay fault testing has also been reported by Motorola for at-speed testing of the high-speed interface between the PowerPC microprocessor and external cache memory [15]. In this application, boundary scan was not implemented, and functional latches were used to implement I/O wrap. I/O wrap can be used regardless whether the pin is contacted or not, both during wafer test and final test.

4. Enhanced Reduced Pin-Count Test

RPCT pays off only if the number of scan data pins is limited. Within Philips, it is common practice to multiplex as many digital IC pins for scan as possible, and a design therefore typically contains as many scan chains as pin-count allows. The advantage of many parallel scan chains is that the scan chains can be shorter which results in shorter test time. Instead of few dedicated tester channels with deep vector memory for the scan data, the normal vector memory behind each tester channel is used to store scan data. In this case, PRCT cannot be used since all pins are used as scan data pins and hence all pins have to be contacted.

A solution is to implement enhanced RPCT, as shown in Figure 2. The basic idea is to load/unload the internal scan chains by using serial/parallel conversion of the test data in the boundary-scan chain. The boundary-scan chain is IEEE 1149.1 compliant, and can be divided into a number of segments for RPCT. A dedicated control scheme is required to control the segments in the boundary-scan chain during RPCT. Test stimuli are loaded serially from the tester into the segments of the boundary-scan chain via the TDI and scan-in pins. Whenever the boundary-scan chain is completely loaded, the data is copied in parallel from the boundary-scan chain into the internal scan chains. This is repeated until the internal scan chains are completely loaded. Also for the scan normal cycle, data is loaded serially from the tester into the segments of the boundary-scan chain, and next the data is copied in parallel from the boundary-scan chain onto the primary inputs of the circuit-under-test (CUT). The test responses are captured in the internal scan chains and in the boundary-scan chain. The test responses are shifted out using parallel-serial conversion in the boundary-scan chain segments.

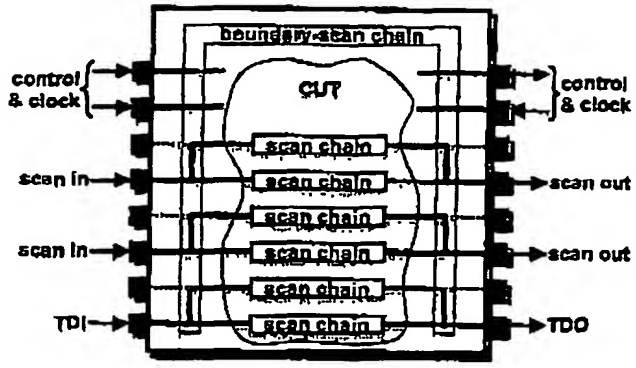

Figure 2: Enhanced reduced pin-count test

The maximum length of the segments in the boundary-scan chains is determined by the ratio of the tester frequency and the internal scan test frequency, as well as the size of the tester vector memory. Test stimuli/responses are serially shifted in/out of the boundary-scan chain segments at the rate of the tester frequency. A typical frequency on data pins of low-cost ATE is 50 MHz. It is not required that the full boundary-scan chain can operate at 50 MHz, which may be difficult to implement. This is required only locally for the individual segments in the boundary-scan chain.

The IC internal scan test frequency is typically 5 to 15 MHz. Scan testing is performed at a low frequency to reduce power dissipation during test, and also since the scan chains and control signals are usually not routed for high speed. In the case where the loading/unloading of segments in the boundary-scan chain is performed at 50 MHz, while the internal scan frequency is 10 MHz, a segment can contain up to 5 cells of the boundary-scan chain, and consequently 5 internal scan chains can be loaded/unloaded in parallel from such a segment. The test application time of enhanced RPCT in this case is similar to the test application time of a traditional test in which all pins are contacted by the tester, and the tester frequency and the internal scan test frequency is 10 MHz.

An additional constraint for enhanced RPCT is that the tester vector memory of the contacted pins should be large enough to store all the test data. Each segment in the boundary-scan chain is serially loaded/unloaded from a single IC pin. In the above case where 5 internal scan chains are loaded from one boundary-scan segment, the vector memory for the contacted pin should be 5 times as large as for traditional, full-contact testing.

A similar concept of on-chip serial/parallel conversion of test data has been presented previously in [16]. However, in [16] test stimuli are loaded in parallel from the tester into a dedicated on-chip buffer, and next data is loaded serially from the buffer into a scan chain. Hence, this approach is opposite to the conversion scheme as used in enhanced RPCT. The goal in [16] is to test a high-speed device on low-speed ATE, which requires many additional pins, while the goal in this paper is to reduce the number of contacted pins in the case of many parallel scan chains.

4.1 Boundary-Scan for Enhanced RPCT

Enhanced RPCT requires that every non-contacted pin is implemented as a bidirectional pin. Figure 3 shows an example boundary-scan cell for such a bidirectional pin. The cell contains two edge-triggered flip-flops, which are clocked at opposite edges of TCK. The shift flip-flop is clocked on the rising edge of TCK, while the update flip-flop is clocked on the negative edge of TCK. The enable signals (en) get a fixed value during RPCT, and the enable signal for multiple pins can be derived from one boundary-scan cell.

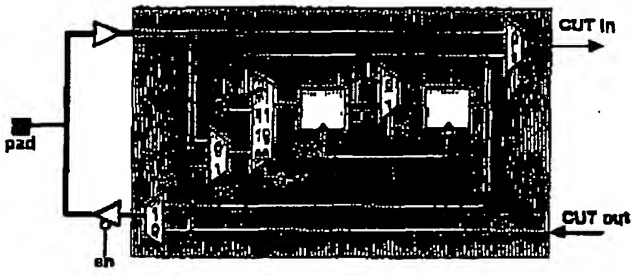

Figure 3: Bidirectional boundary-scan cell

The boundary-scan cell in Figure 3 can be configured into various operation modes by means of the multiplexers and the control signals c0-c5. In shift mode (c0-c1=11), data is shifted in/out of the shift flip-flop via the scan data input (si) and scan data output (so). In update mode (c2=1), data is copied from the shift flip-flop into the update flip-flop. In capture mode (c0-c1=00), functional data is loaded into the shift flip-flop. In hold mode (c0-c1=01, c2=0), the flip-flops hold their data values by capturing their own outputs.

An IC with boundary scan and enhanced RPCT can operate either in application mode, in boundary-scan test mode according to IEEE 1149.1, or in enhanced RPCT mode. Figure 4 shows symbolically the configuration of the boundary-scan cells during serial/parallel conversion. Each of the figures shows a segment of the boundary-scan chain containing three boundary-scan cells. A segment is loaded/unloaded serially from one IC pin.

- Figure 4a) shows the configuration of a segment at the input side, when serially shifting in test data from the IC pin. The shift flip-flops are configured into a shift register, while the update flip-flops operate in hold mode to provide stable data to the CUT.

- Figure 4b) shows the configuration of the segment when the update flip-flops are loaded in parallel from the shift flip-flops. The data is output to the CUT, and is either copied to the scan chains during scan shifting or to the CUT's functional inputs during the scan normal cycle.
- Figure 4c) shows the configuration of a segment at the output side, when data is captured in parallel into the shift register from the CUT. The data is either the responses at the CUT's primary outputs during the scan normal cycle, or data shifted out of the scan chains during scan shifting.
- Figure 4d) shows the configuration of the segment when serially shifting out data on the IC pin. Only the update flip-flop at the contacted pin is used.

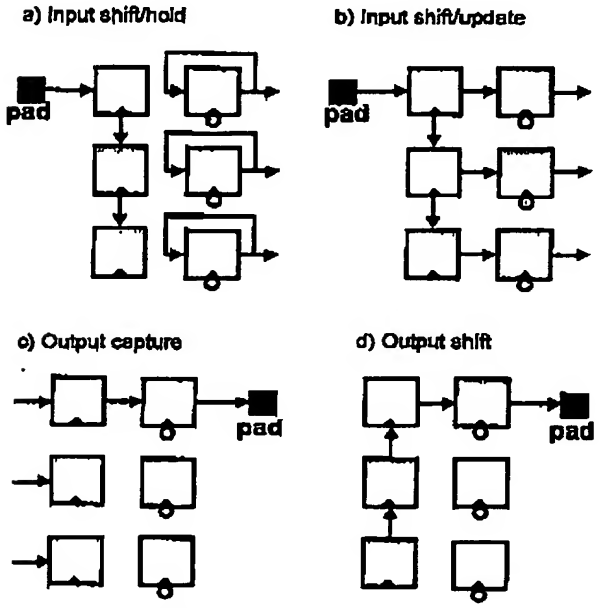

Figure 4: Serial/parallel conversion

IC pins that are functionally bidirectional contain three boundary-scan cells (that differ from Figure 3): one cell for the input, one cell for the output, and one cell for control. With enhanced RPCT, the boundary-scan cell for the input should be part of a boundary-scan chain segment at the input side (Figure 4a and b), while the boundary-scan cells for output and control should be part of segments at the output side (Figure 4c and d).

The control scheme for enhanced RPCT differs from the standard boundary-scan control scheme. The control signals for the boundary-scan cells during enhanced RPCT are listed in Table 1. The value 'U' for signal c2 at the input cells controls whether the update flip-flops operate in hold mode or captures data from the shift flip-flops, as depicted in the timing diagram in Figure 5. The value 'C' for the signals c0 and c1 at the output cells controls whether the shift flip-flops operate in shift mode or capture data from the CUT, as depicted in the timing diagram in Figure 6.

Contacted input	c0	c1	c2	c3	c4	c5
Functional mode	-	-	-	0	0	-
Enhanced RPCT	0	0	U	-	1	0

Uncontacted input	c0	c1	c2	c3	c4	c5
Functional mode	-	-	-	0	0	-
Enhanced RPCT	1	1	U	-	1	-

Contacted output	c0	c1	c2	c3	c4	c5
Functional mode	-	-	-	0	0	-
Enhanced RPCT	C	C	1	1	-	1

Uncontacted output	c0	c1	c2	c3	c4	c5
Functional mode	-	-	-	0	0	-
Enhanced RPCT	C	C	-	-	-	1

Table 1: Control for boundary-scan cells

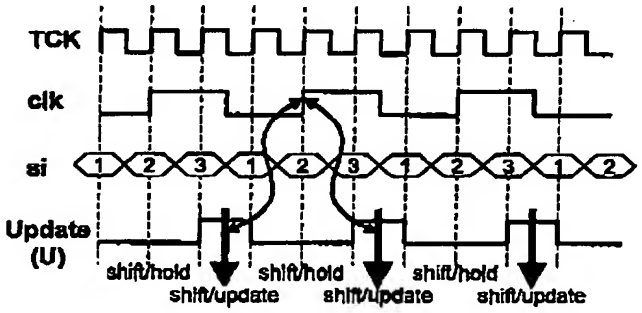

Figure 5: Timing diagram for serial/parallel conversion

In the timing diagram in Figure 5, the shift flip-flops capture scan-in data (si) at the positive edge of TCK. The update flip-flops capture data at the negative edge of TCK, and they operate either in hold mode or capture data from the shift flip-flops as controlled by the update signal. The CUT is clocked by the internal test clock clk. Data transfer from the boundary-scan chain to the CUT therefore implies communication between two different clock domains, and the clocks TCK and clk should be synchronized. As explained previously, TCK runs at the tester frequency, and is a multiple of the internal scan test frequency clk. The ratio of the clock frequencies of TCK and clk determines the size of the segments in the boundary-scan chain (which is 3 in the example in Figure 5). As shown in Figure 5, the update signal provides a clock skew margin of 3 cycles of clock TCK. In case of TCK running at 50 MHz, the skew margin is 60 ns, which is large enough to prevent clock skew problems even if the clocks are not balanced at top-level.

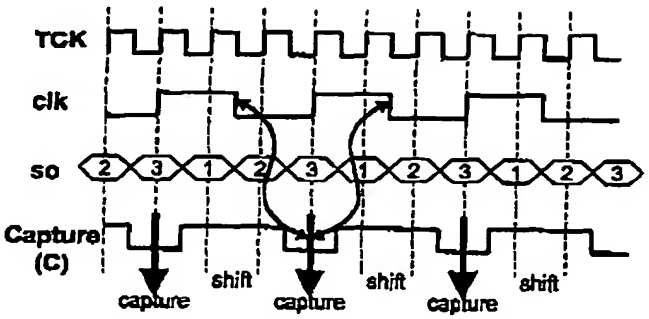

Figure 6: Timing diagram for parallel/serial conversion

The timing diagram in Figure 6 shows a similar situation at the output side. The shift flip-flops capture data at the positive edge of TCK, and they operate either in shift mode or capture data from the CUT as controlled by the capture signal. The CUT is clocked by the internal test clock clk, and data appears at the outputs of the internal scan chains at the falling edge of clk. Also in this case, the capture signal provides a skew margin for the clocks TCK and clk of 3 cycles of clock TCK. The update flip-flops capture data at the negative edge of TCK, and this data is observed as scan-out data (so) at the IC pins.

4.2 I/O wrap

The boundary-scan chain is also used to perform an I/O wrap test. During I/O wrap test, test stimuli are shifted into the boundary-scan chain via input TDI, and the responses are shifted out via output TDO. During the capture cycle, the bidirectional boundary-scan cells of the uncontacted pins perform an I/O wrap test. The signal path during the I/O wrap test is indicated in bold in Figure 3.

5. Enhanced RPCT and Core-Based Test

Enhanced RPCT can also be used for full-scan, core-based design, but this requires some modifications to the enhanced RPCT scheme. Enhanced RPCT for core-based design allows improved I/O wrap tests.

5.1 Core-Based Test

Key concepts in testing of core-based designs are the test access mechanism (TAM) and wrapper [17][18], as shown in Figure 7. The wrapper around a core contains a surround scan chain to isolate all functional core I/Os during test. The TAM provides access from the IC pins to the core wrapper during test. The wrapper connects the TAM to the surround scan chain and the internal scan chains.

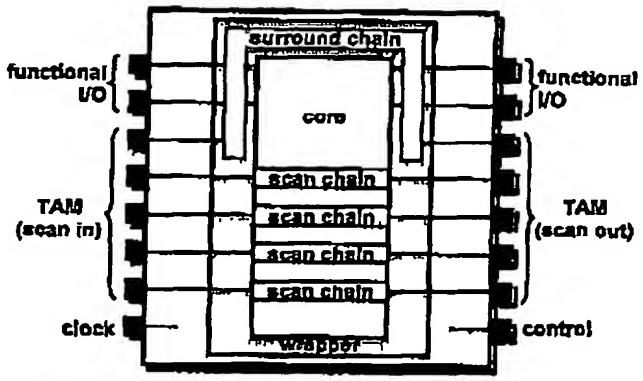

Figure 7: Connections between core and IC pins

The TAM and wrapper can be configured by appropriate test control into the following modes:

1. *Functional mode* during normal operation, in which the wrapper is transparent and the IC is not tested.
2. *Core-test mode* to test the internals of the core. The wrapper is used to isolate the core from its surrounding. Test data is transported via the TAM to the wrapper. The wrapper takes care that test stimuli are applied to the core via the surround chain and the scan chains, and that responses are captured in the surround chain and the scan chains.
3. *Interconnect-test mode* to test the interconnections between the cores, between the cores and the IC pins, and possibly glue logic. The TAM is used to transport test data between the IC pins and the wrapper. The surround chain is configured to apply test stimuli to the surrounding of the core, and to capture test responses of tests originating from the IC pins and from wrappers of other cores in the surrounding.

5.2 Enhanced RPCT

The basic idea of enhanced RPCT for core-based test is to load/unload the scan chains by using serial/parallel conversion of the test data in the boundary-scan chain. Also in this case, it is common practice within Philips to multiplex all digital IC pins for scan. Hence, the width of the TAM is as large as pin-count allows.

The advantages of enhanced RPCT with core-based test is that the I/O wrap test can be part of the interconnect test, and does not require separate test patterns. Furthermore, the I/O wrap test performs a complete test of the functional path between the boundary-scan chain and the surround chain.

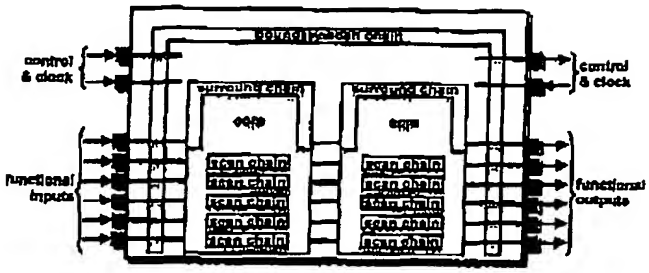

Figure 8: Functional mode

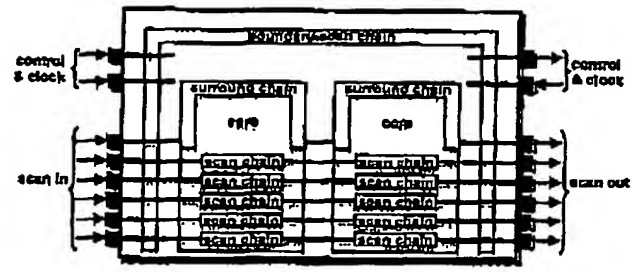

Figure 9: Standard core test

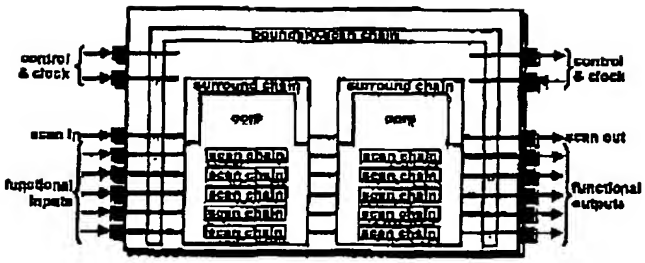

Figure 10: Standard interconnect test

Figure 8 shows an example IC containing two cores. In functional mode, all IC data pins are used as functional I/Os. Figure 9 shows the configuration for standard core-test mode in which all pins are contacted by the tester. All digital IC pins are multiplexed for scan, and hence all digital data pins are used to load/unload the surround chains and the scan chains. Figure 10 shows the configuration for standard interconnect-test mode. During interconnect test, the cores are treated as black boxes, and only the surround chains are involved in the test. The connections between the cores, and the connections between the cores and the IC pins are tested.

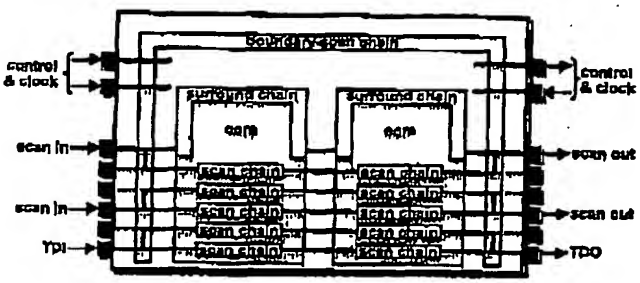

Figure 11: Enhanced RPCT core test

Figure 11 shows the configuration for the core-test mode with enhanced RPCT. The boundary-scan chain is IEEE 1149.1 compliant, and can be divided into a number of segments for RPCT. Only the scan in/out pins of the segments are actually connected to the tester, and all other scan data pins are not contacted. Test stimuli are loaded serially from the tester into the segments of the boundary-scan chain via the TDI and scan-in pins. Whenever the boundary-scan chain is completely loaded, the data is copied in parallel from the boundary-scan chain segments into the scan chains. This is repeated until all scan chains are completely loaded.

In the scan normal cycle, test stimuli are applied from the surround chains and the scan chains, and test responses are captured in the surround chains and the scan chains. The test responses are transported to the IC pins using parallel-serial conversion in the segments of the boundary-scan chain. The outputs of the scan chains are copied in parallel to the boundary-scan chain segments, and the data is next shifted out serially to the IC pins. This is repeated until all scan chains are completely unloaded. As for standard scan test, new test stimuli can be shifted into the scan chains while shifting out the test responses.

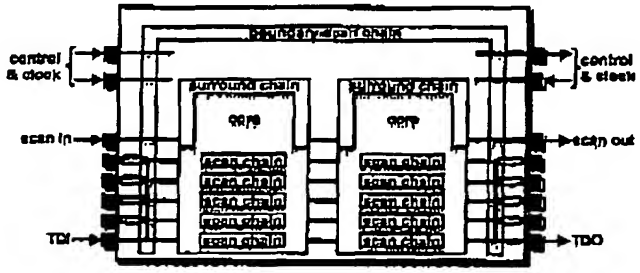

Figure 12: Enhanced RPCT interconnect test

Figure 12 shows the configuration for the interconnect-test mode with enhanced RPCT. The boundary-scan chain is not divided into segments for the interconnect test. The TDI and TDO pins of the boundary-scan chain are used to load/unload the boundary-scan chain, and hence these pins should be connected to the tester. Also

the scan input and scan output of the surround chains should be connected to the tester. Test stimuli are shifted in serially from the contacted IC pins into the boundary-scan chain and the surround chains. The boundary-scan chain and the surround chains all operate at the same clock frequency.

During the scan normal cycle, the test responses are captured in the boundary-scan chain and the surround chains. Next the test responses are shifted out via the contacted scan output pins, and simultaneously new test stimuli are shifted in via the contacted scan input pins.

In the scan normal cycle, an I/O wrap test is performed on all uncontacted pins (denoted by the ellipses in Figure 12). To accommodate I/O wrap testing, all uncontacted pins should be implemented as bidirectional pins. During I/O wrap testing, a test stimulus is launched from the update flip-flop in the boundary-scan cell, and the response is captured in the surround chain, as depicted in Figure 13. For output paths, a test stimulus is launched from the surround chain, and the response is captured in the shift flip-flop of the boundary-scan cell, as depicted in Figure 14. The I/O wrap test now also covers the functional path between driver/receiver and the surround scan chain.

Figure 13: I/O wrap test on input path

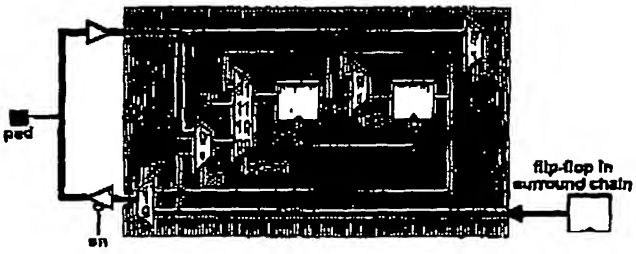

Figure 14: I/O wrap test on output path

6. Tooling Issues

Enhanced RPCT requires tool support for generating the boundary-scan hardware with a segmented boundary-scan chain and the control scheme, as well as for generating appropriate test patterns and test protocols. The tool flow for enhanced RPCT is outlined in Figure 15. The ATPG tool generates test patterns for testing the cores and the interconnect. Test protocol expansion is used for transforming the test protocols from the core terminals to the IC pins. A test protocol defines how to apply the test patterns. The test patterns contain the actual test stimuli and responses, while the test protocols contain control information for how to apply the test patterns. The test assembly tool assembles the test patterns and the test protocols into a complete test. For enhanced RPCT, a conversion tool is required to adjust the test protocols for the serial/parallel conversion in the boundary-scan chain segments.

The boundary-scan generator creates a description of the boundary-scan hardware. The boundary-scan hardware includes support for the boundary-scan chain segments and the control scheme. The tool also generates an 'enhanced RPCT view', which contains the configuration of the boundary-scan chain segments for enhanced RPCT. This view is used by the conversion tool the adjust the test protocols.

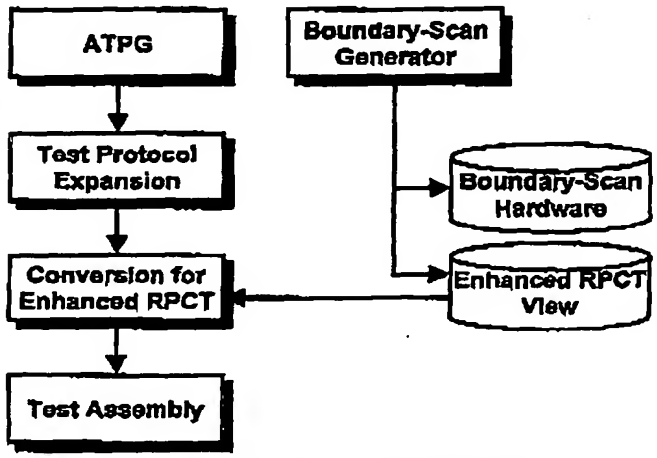

Figure 15: Tool flow for enhanced RPCT

References

[1] Semiconductor Industry Association (SIA), *International Technology Roadmap for Semiconductors (ITRS)*, 1999 edition, 2000 update.

[2] Panel session, *DFT-focused chip testers: what can they really do?*, Proceedings International Test Conference, IEEE, 2000, pp. 1119-1122.

[3] Y. Zorian, *Testing the monster chip*, IEEE Spectrum, July 1999, pp. 54-60.

[4] N. Zacharia, J. Rajski, J. Tyszer, *Decompression of test data using variable-length seed LFSRs*, Proceedings VLSI Test Symposium, IEEE, 1995, pp. 426-433.

[5] A. Jas, N.A. Touba, *Test vector decompression via cyclical scan chains and its application to testing core-based designs*, Proceedings International Test Conference, IEEE, 1998, pp. 458-464.

[6] A. Jas, J. Ghosh-Dastidar, N.A. Touba, *Scan vector compression/decompression using statistical coding*, Proceedings VLSI Test Symposium, IEEE, 1999, pp. 114-120.

[7] A. Chandra, K. Chakrabarty, *Test data compression for system-on-a-chip using Golomb codes*, Proceedings VLSI Test Symposium, IEEE, 2000, pp. 113-120.

[8] R.W. Basset et al., *Low cost testing of high density logic components*, Proceedings International Test Conference, IEEE, 1989, pp. 550-557.

[9] R.W. Basset et al., *Boundary-scan design principles for efficient LSSD ASIC testing*, IBM Journal on Research and Development, Vol. 34 (1990), No. 2/3, pp. 339-354.

[10] P.S. Gillis, T.S. Guzowski, B.L. Keller, R.H. Kerr, *Test methodologies and design automation for IBM ASICs*, IBM Journal on Research and Development, Vol. 40 (1996), No. 4, pp. 461-474.

[11] W.V. Huott et al., *Advanced microprocessor test strategy and methodology*, IBM Journal on Research and Development, Vol. 41 (1997), No. 4/5, pp. 611-628.

[12] T.G. Foote et al., *Testing the 500-MHz IBM S/390 Microprocessor*, IEEE Design & Test of Computers, July-September 1998, pp. 83-89.

[13] *IEEE Standard test access port and boundary-scan architecture*, IEEE Std. 1149.1, 1990.

[14] P. Gillis, F. Woytowich, K. McCauley, U. Baur, *Delay test of chip I/Os using LSSD boundary scan*, Proceedings International Test Conference, IEEE, 1998, pp. 83-90.

[15] N. Tendolkar, R. Molyneaux, C. Pyron, R. Raina, *At-speed testing of delay-faults for Motorola's MPC7400, a PowerPC Microprocessor*, Proceedings VLSI Test Symposium, IEEE, 2000, pp. 3-8.

[16] D. Heidel et al., *High speed serializing/de-serializing design-for-test method for evaluating a 1 GHz microprocessor*, Proceedings VLSI Test Symposium, IEEE, 1998, pp. 234-238.

[17] Y. Zorian, E.J. Marinissen, S. Dey, *Testing Embedded-Core Based System Chips*, Proceedings International Test Conference, IEEE, 1998, pp. 130-143.

[18] E.J. Marinissen, R. Kapur, Y. Zorian, *On Using IEEE P1500 SECT for Test Plug-n-Play*, Proceedings International Test Conference, IEEE, 2000, pp. 770-777.

CLAIMS:

1. Method for testing an integrated circuit with a surrounding scan chain, said scan chain being connected to an external test device by a test data in pin and a test data out pin, said circuit further comprising a first and a second internal scan chain, said method comprising the following steps:

- shifting a first and a second input data element from the test device through the test data in pin on a first segment of the surrounding scan chain in a serial fashion;
- shifting the first input data element from the first segment of the surrounding scan chain into the first internal scan chain and shifting the second input data element from the first segment of the surrounding scan chain into second internal scan chain in a parallel fashion;
- shifting a first output data element from the first internal scan chain and a second output data element from the second internal scan chain onto a second segment of the surrounding scan chain in a parallel fashion;
- shifting the first and second output data element from the second segment of the surrounding scan chain through the test data out pin on the test device in a serial fashion.

2. Integrated circuit, comprising:

- a first internal scan chain;
- a second internal scan chain;
- a first data in pin;
- a first data out pin;
- a surrounding scan chain comprising:
  - a first segment, connected to the first internal scan chain through a first scan cell and to the second internal scan chain through a second scan cell;
  - a second segment connected to the first and second internal scan chain,

    wherein:
- the first data in pin is connected to the external test device and to the first segment of the surrounding scan chain;

– the first data out pin is connected to the external test device and to the second segment of the surrounding scan chain;

and wherein said surrounding scan chain is arranged to feed a first data element to the first internal scan chain and a second data element to the second internal scan chain in a parallel fashion.

3. An integrated circuit according to claim 2, in which the surrounding scan chain is a boundary scan chain.

4. An integrated circuit according to claim 2 or 3, further comprising:

– a second data in pin;
– a second data out pin;
– a third internal scan chain;
– a fourth internal scan chain;

in which the surrounding scan chain further comprises:

– a third segment connected to the third internal scan chain through a third scan cell and to the fourth internal scan chain through a fourth scan cell;
– a fourth segment connected to the third and fourth internal scan chain,

wherein:

– the second data in pin is connected to the external test device and to the third segment of the surrounding scan chain;
– the second data out pin is connected to the external test device and to the fourth segment of the surrounding scan chain;

and wherein said surrounding scan chain is arranged to feed a third data element to the third internal scan chain and a fourth data element to the fourth internal scan chain in a parallel fashion.